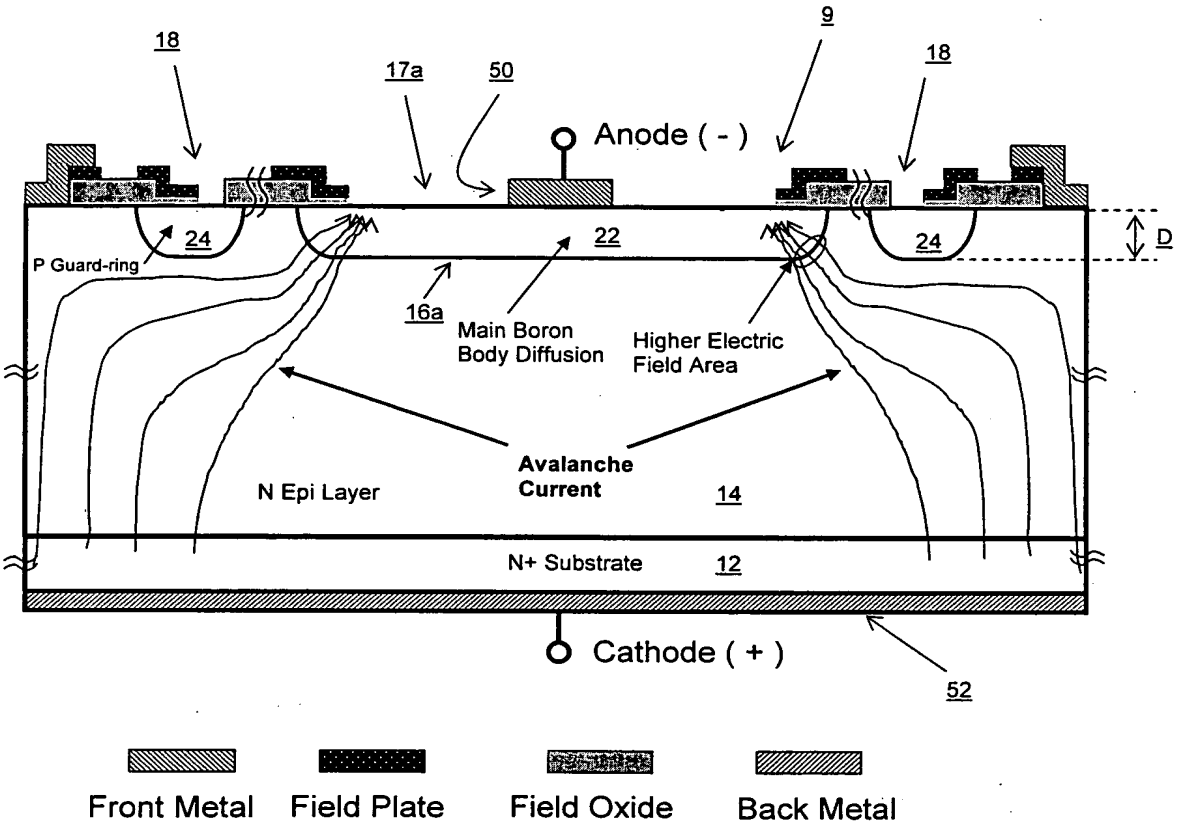
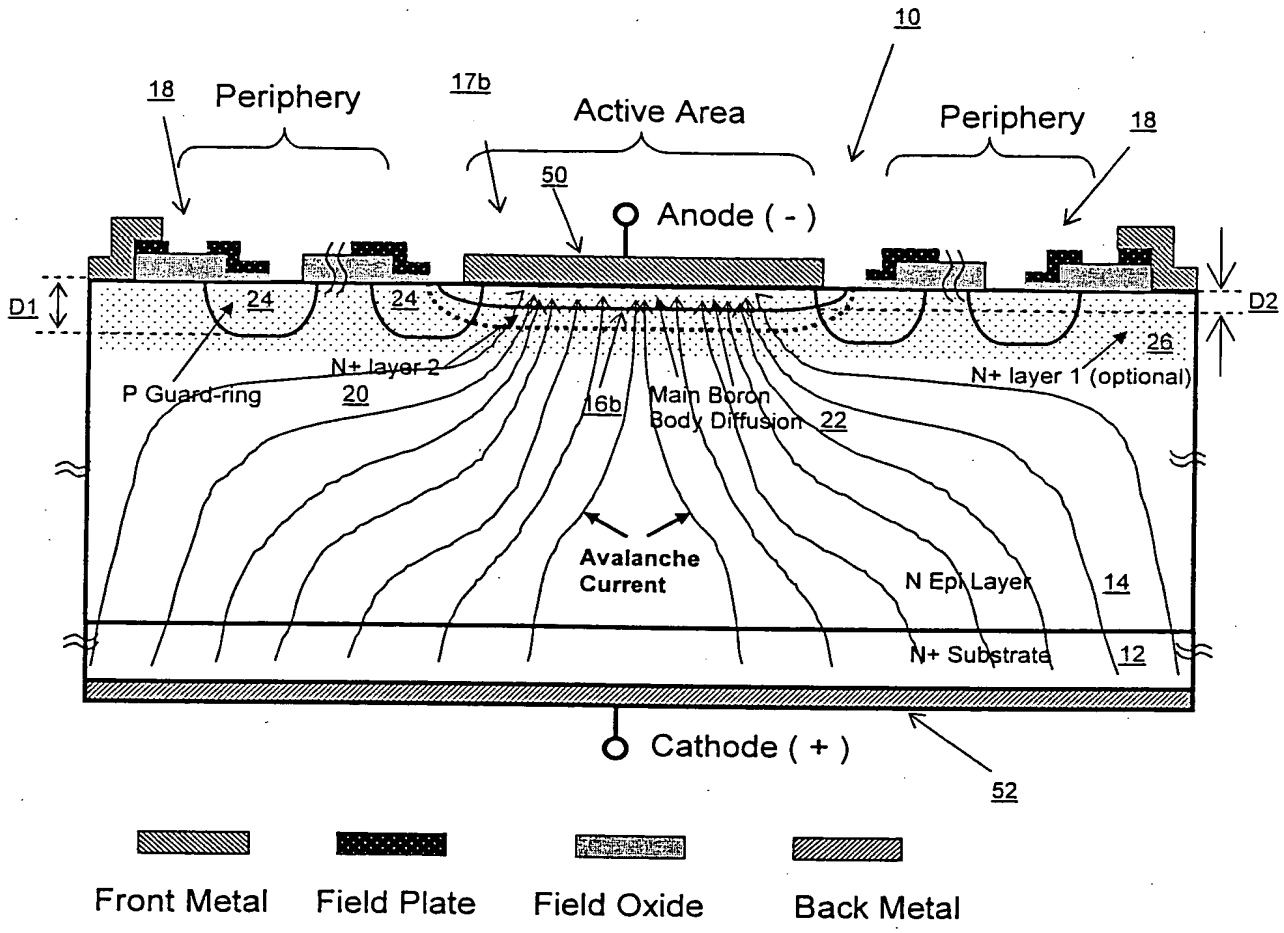


Prior Art Device

Figure 1(a) Avalanche current flow in a prior art device.



Present Invention Device

Figure 1(b) Avalanche current flow of the present invention.

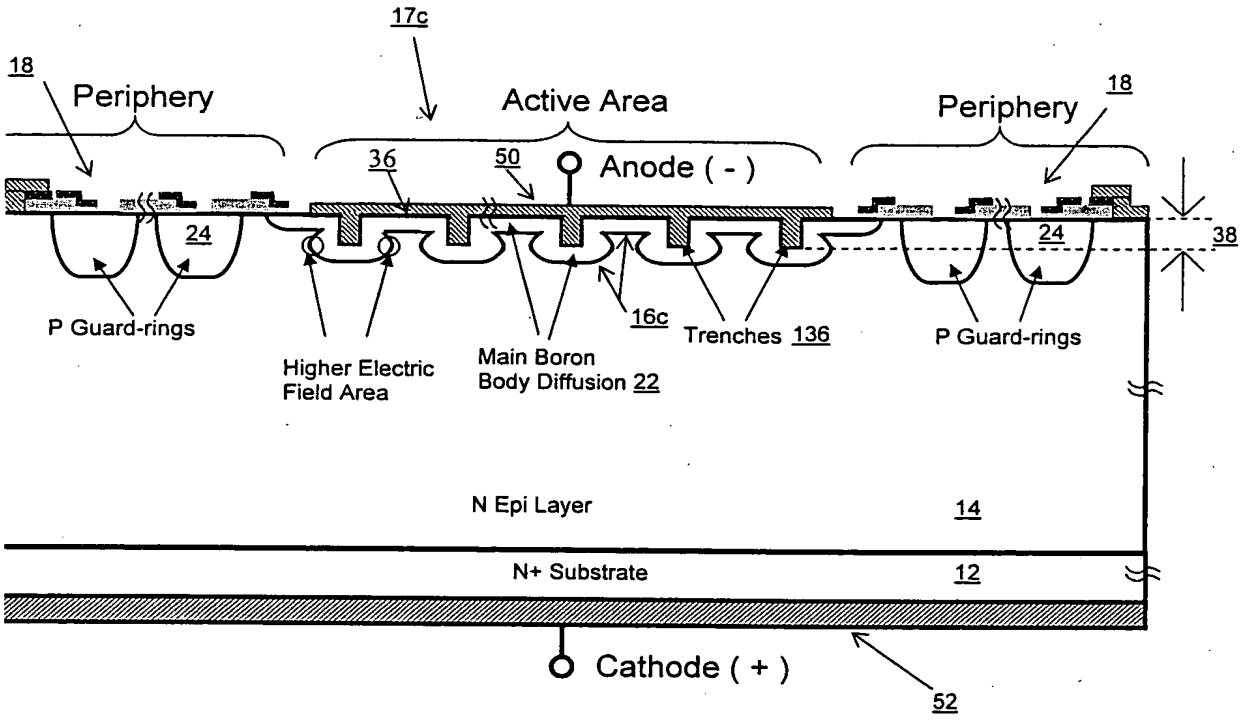


Figure 2(a) Cross-sectional view of a FRED with trenched active area.

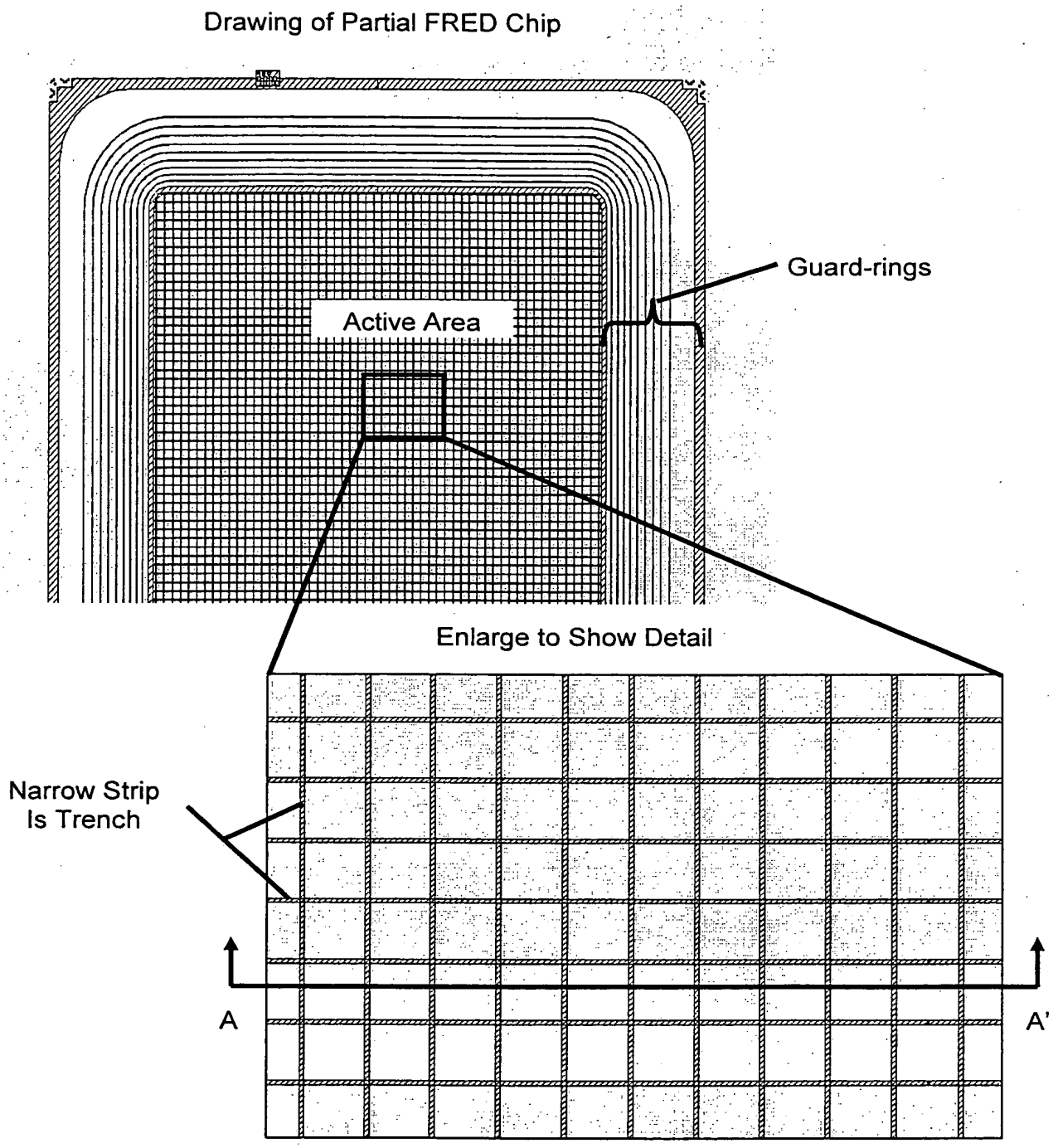


Figure 2(b) Top view of a representative "grid" type trench layout for a rugged FRED. A cross-sectional view along line AA' gives the view shown in Figure 2(a). Other trench patterns are obvious to one skilled in the art.

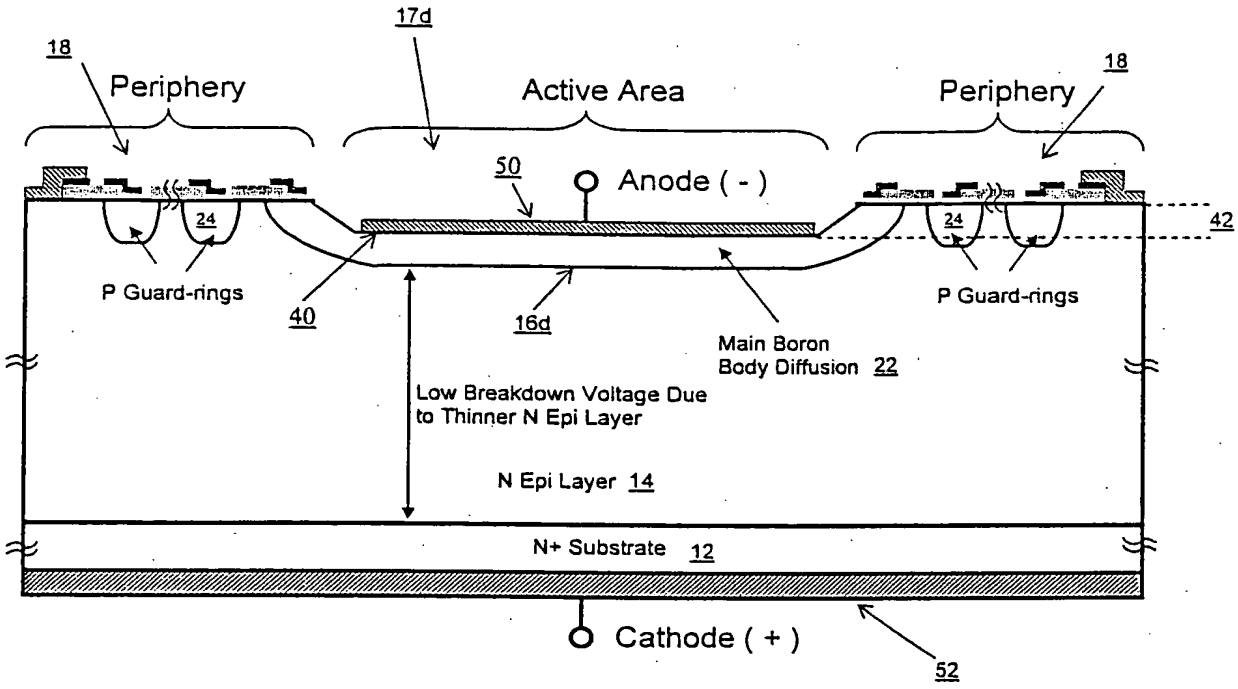


Figure 3 Cross-sectional view of a FRED with thinner active area.

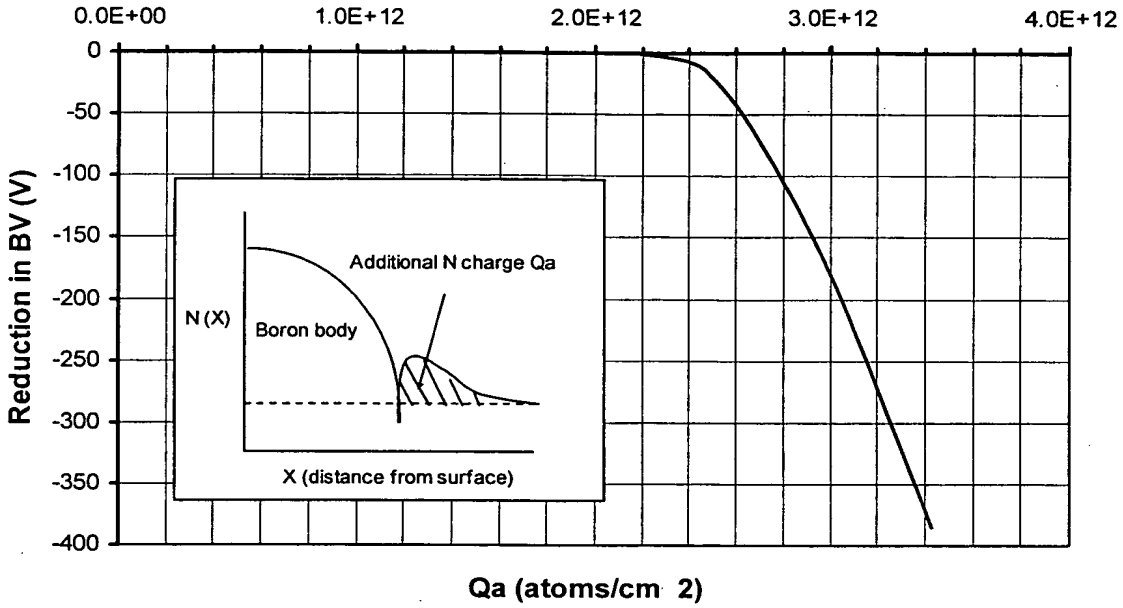
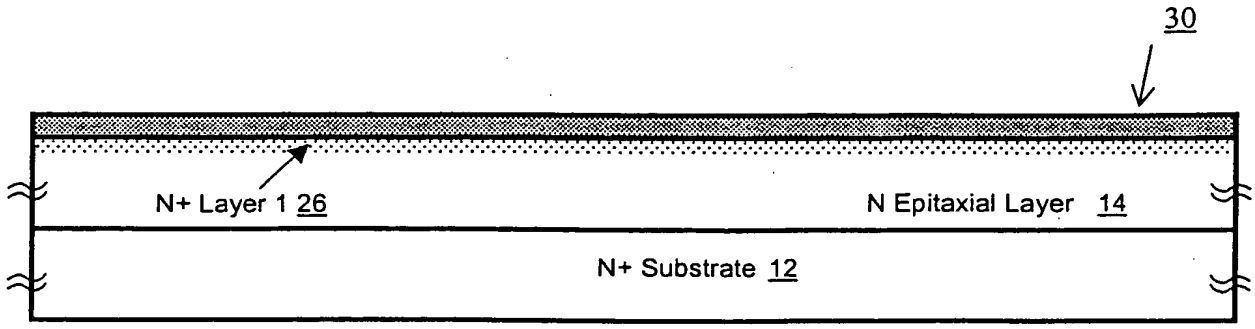
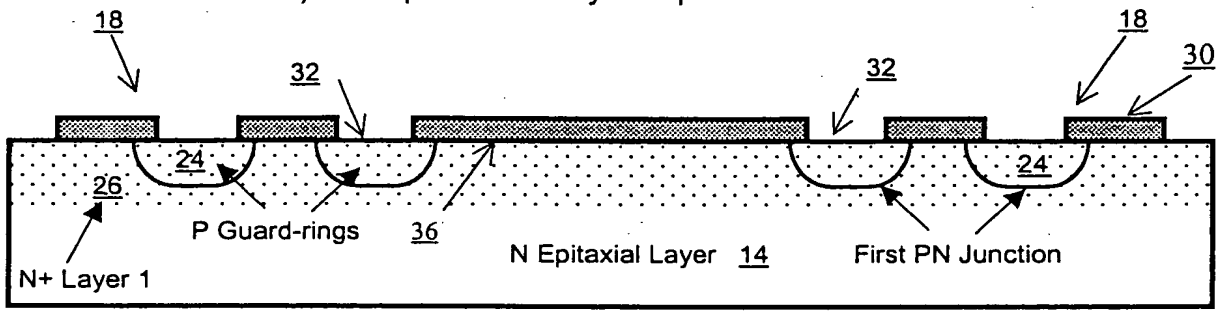


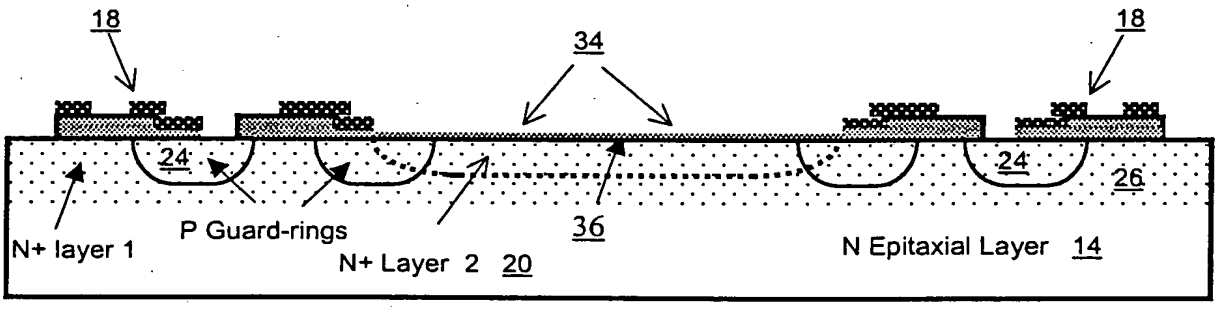
Figure 4 Breakdown voltage reduction vs. calculated additional N-charge. (Net charge may be reduced by the life-time control process.)



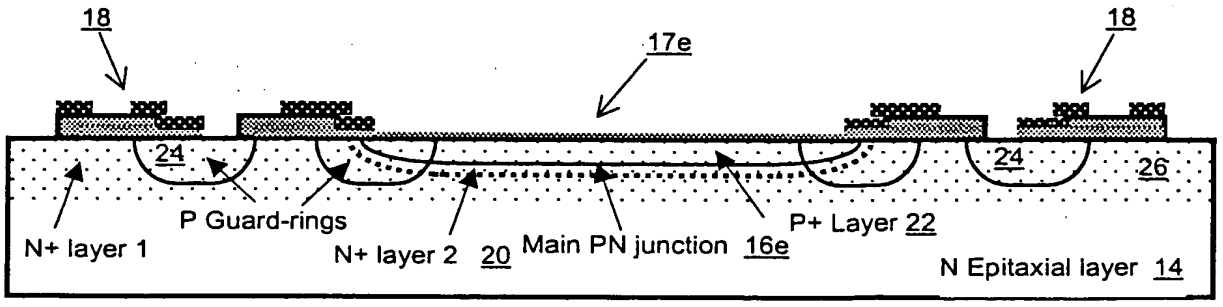
a) Optional N+ layer implant over entire wafer.



b) Pattern and diffuse guard-ring boron and optional N+ Layer.



c) N+ layer implant and diffusion in active area.



d) Shallow P layer implant and diffusion in active area.

Figure 5

Key process steps for a device corresponding to the principle showing in Figure 4.
(The N+ substrate layer 12 has been omitted for convenience in Figures 5(b)-5(d).)

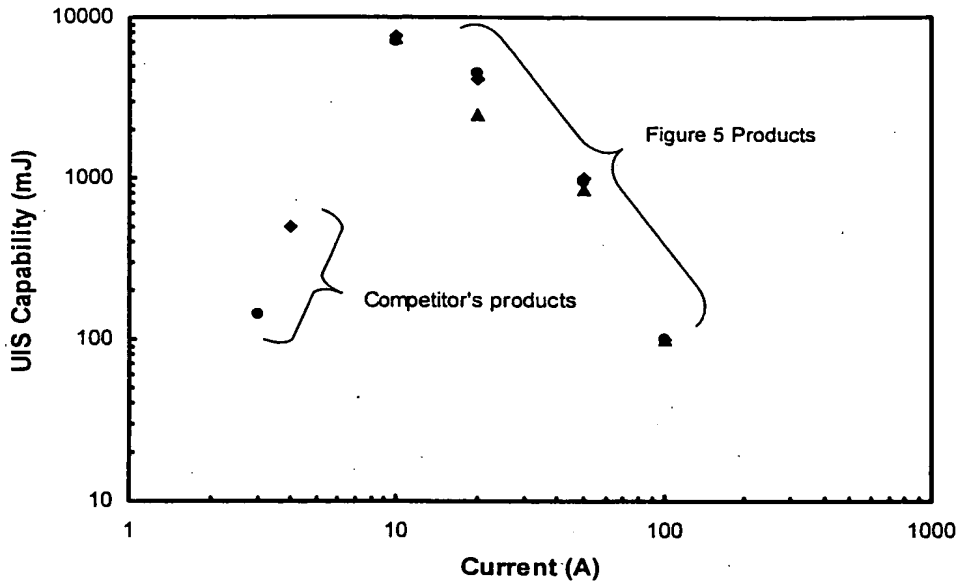


Figure 6 Comparison of UIS energy capability versus avalanche current.

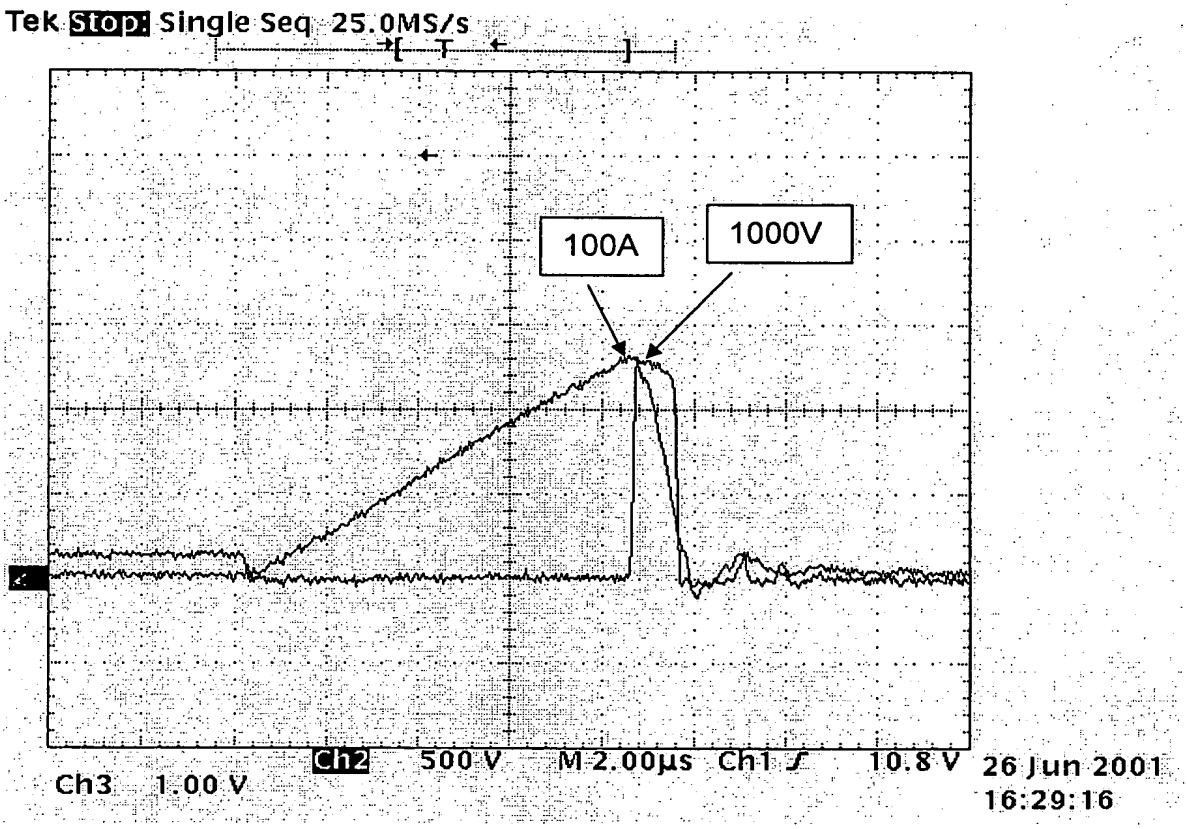


Figure 7 Typical UIS test waveform for a rugged FRED.

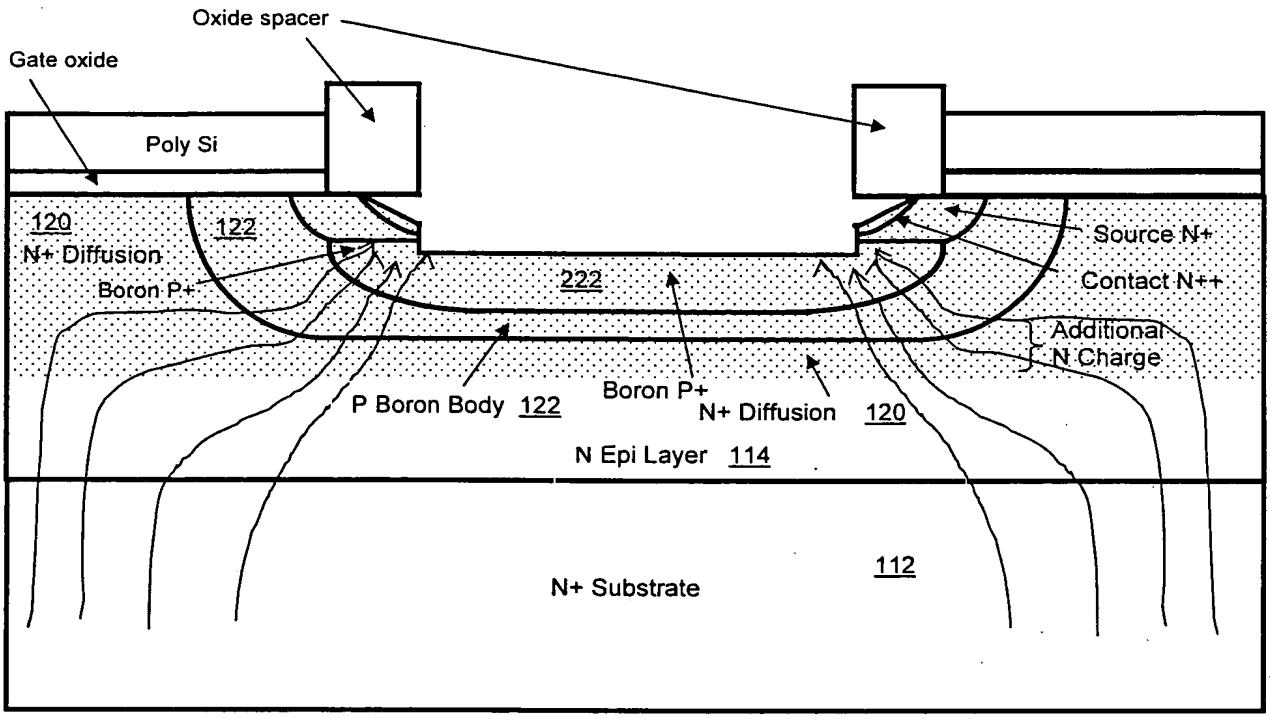


Figure 8(a) Avalanche of the P-body - N+ diffusion junction of a MOSFET induced by introducing additional N-charge underneath the PN junction.

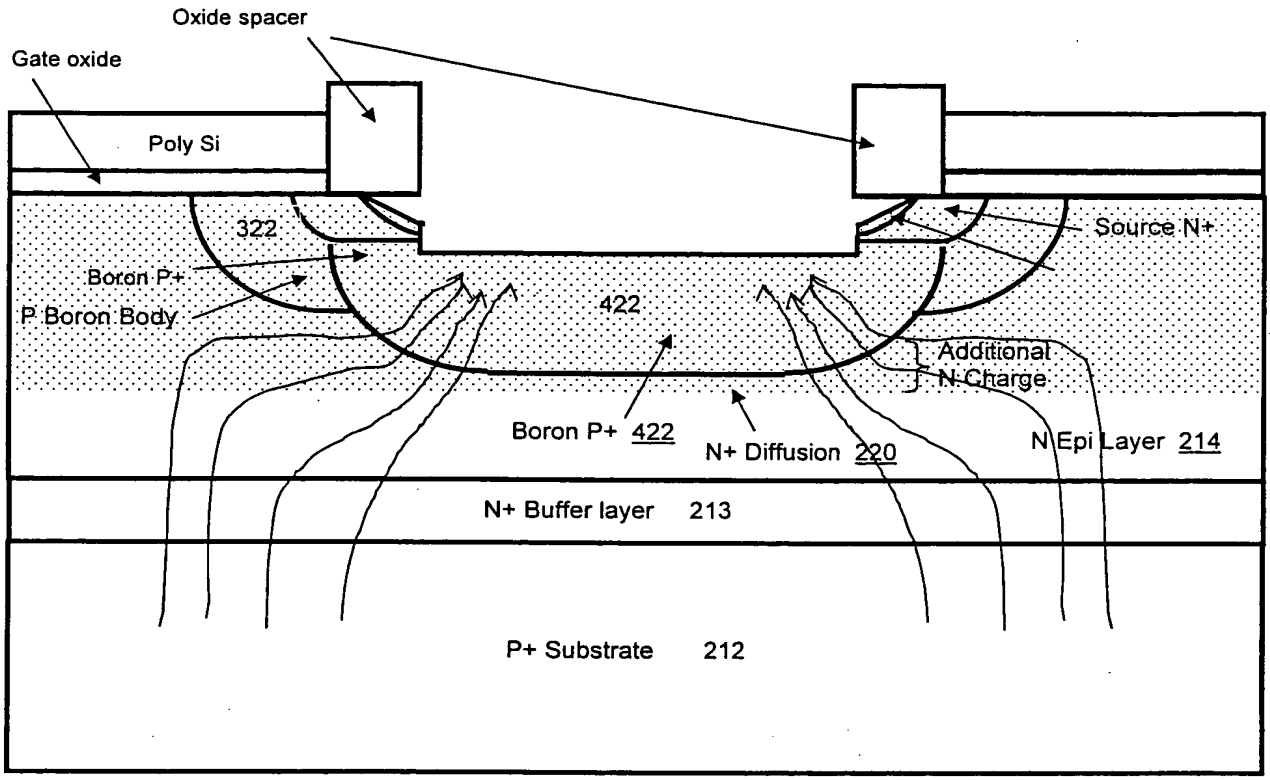


Figure 8(b) Avalanche of the P+ - N+ diffusion junction of an IGBT induced by introducing additional N-charge underneath a deep PN junction.

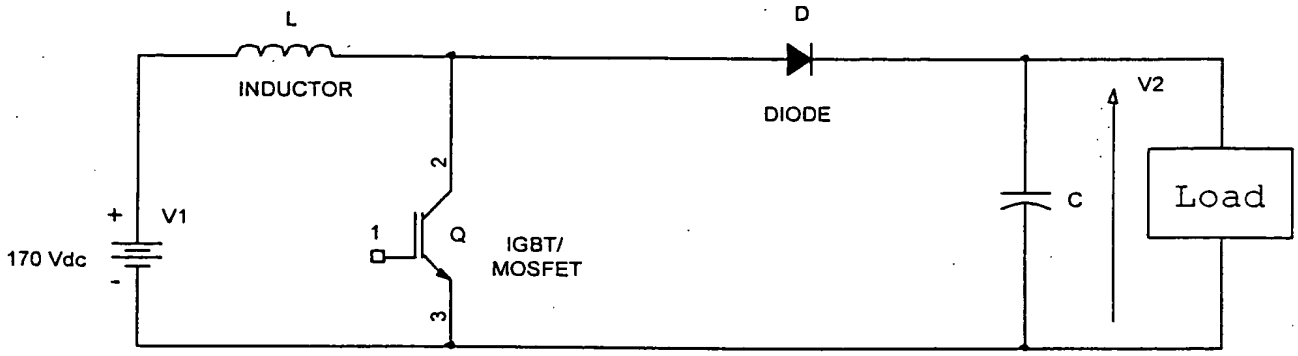


Figure 9 A common boost circuit using one power switch and one diode. A rugged diode in this circuit will improve system reliability and allows operation closer to the diode avalanche voltage.